William Wong

willwong812@gmail.com | 312-678-9779 | U.S. Citizen | Hinsdale, IL

Education

University of Illinois Chicago, College of Engineering - Chicago, IL

Master of Science in Computer Engineering - 2027

Purdue University, College of Engineering - West Lafayette, IN

Bachelor of Science in Computer Engineering - 2025

Relevant Coursework: ASIC Design Lab, Systems And Signals, Artificial Intelligence, Data Structures, Computer Design and Prototyping, Compiler Systems, Object-Oriented Programming with C++, Computer Security, Operating Systems Engineering

Research Experience - See will-wong.com for a compilation of all my projects/research.

Purdue SoCET - Purdue Universitv

Undergraduate Researcher

- Led a team of 3 undergraduate students on the design of a memory subsystem for a Systolic Array, leveraging insights from the • Gemmini and RASA papers to accelerate AI computations and optimize design architecture.
- Designed parametric I-Cache, D-Cache, scratchpad, and memory arbiter to be able to handle memory requests for both scalar and matrix operations.
- Synthesized the scratchpad using MITLL's 90 nm Silicon-on-Insulator process and achieved a clock frequency of 696MHz over a • 1Ghz clock, demonstrating high throughput.

Projects

CIFAR-10 Image Classifier with PyTorch - My Demo

- Spring 2025 Created multiple image predictors using different neural network models in order to teach undergraduate students an introduction to neural network applications in practice.
- Organized the procedure to build a CNN to handle images from the CIFAR-10 dataset, achieving a final test accuracy of 90.09%. •
- Produced an .ipynb to TSX Python script to convert an interactive coding space like Google Colab or Jupyter into a webpage. •

AES-256 Implementation with CTR Mode and X9.31 Extensions - My Demo

- Spring 2025 Built an AES-256 encryption class in Python, using the Bitvector library, in order to encrypt PPM images and to generate • pseudorandom numbers.
- Converted a Python script into a detailed Jupyter notebook with markdown and code cells to showcase the encryption process such as: • substituting each byte, shifting a row of bytes, mixing columns with matrix multiplication, and adding the round keys.

Dual Core Pipelined RISC-V Processor

- Fall 2024 Prototyped modules with RTL designs and an FPGA respectively, that individually controlled the memory caches, datapath, and signals for the processor to handle RISC-V instructions.
- Conducted detailed waveform analyses on system processors, analyzing key metrics such as maximum frequency and CPI for • calculations and achieving a 628% speedup in total execution time compared to a single-cycle, non-cached, non-pipelined processor.
- Synthesized and optimized a multicore, pipelined processor by improving module pathways and timing, achieving top 5 performance • in frequency and CPI among 200 classmates.

USB AHB-Lite SoC Module

- Coordinated version control processes with Git to document the development progress of RX, TX, and AHB-Lite modules for USB data packet parsing and handshaking.
- Developed AHB-Lite bus interface logic to enable efficient register access and DMA-based data transfers between USB endpoints and • on-chip memory, reducing CPU overhead by 62%.

Audio Equalizer Project

- Designed and prototyped an analog audio equalizer on a breadboard, integrating low-pass, high-pass, and band-pass filters to tune bass (up to 320 Hz), mid (0.32–3.2 kHz), and treble (above 3.2 kHz) frequency bands.
- Implemented low-noise amplifiers (LF356N) and a summing amplifier (LM324) for volume control, achieving 108 mV RMS (+8% • increase over expected value of 100mV) output at maximum settings and <15 mV RMS at minimum.

Work Experience

RS Five. LLC

Community Outreach Subcontractor

Collaborated within a mentored team to engage community members and guide homeowners through the process of replacing • damaged property from severe storms.

Skills

Fall 2023

Fall 2022

Glenview. IL

May 2025 - Present

August 2024 - May 2025

West Lafayette, IN